design ideas

Edited by Bill Travis and Anne Watson Swager

Model a nonideal transformer in Spice

Vittorio Ricchiuti, Siemens ICN, L'Aquila, Italy

DESIGNERS OFTEN USE transformers as voltage, current, and impedance adapters. Transformers usually comprise two inductively coupled coils, wound around a ferrite core. The coupling between the windings is never perfect. Spice provides a model (**Figure 1a**) of the coupled inductors using the k parameter, which is the coefficient of coupling between the windings. The model takes into account self and mutual inductances. With nonideal transformers, the problem is to determine k. **Figure 1b** shows a proposed equivalent circuit of a nonideal transformer, in which the conduction losses in the windings and the core losses are assumed to be negligible. L_S is the equivalent leakage inductance of the transformer, L_P is its magnetization inductance, and T is an ideal transformer (k=1) with transformation ratio equal to n. To obtain equivalence between the two circuits in **Figure 1**, we consider the equations describing these circuits. For the circuit in **Figure 1a**, the expressions are

$$V_1 = j\omega L_1 I_1 + j\omega M I_2;$$

$$V_2 = j\omega M I_1 + j\omega L_2 I_2.$$

For the circuit in **Figure 1b**, the equations are

$$V_1 = j\omega\left(L_S + L_P\right) I_1 + j\omega L_P \frac{I_2}{n};$$

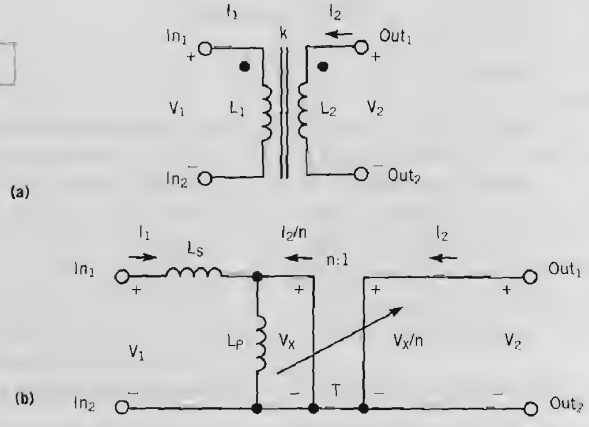
$$V_2 = j\omega \frac{L_P}{n} I_1 + j\omega \frac{L_P}{n^2} I_2.$$

Comparing the two systems and considering $M = k(L_1 L_2)^{1/2}$, we obtain

$$L_1 = L_S + L_P;$$

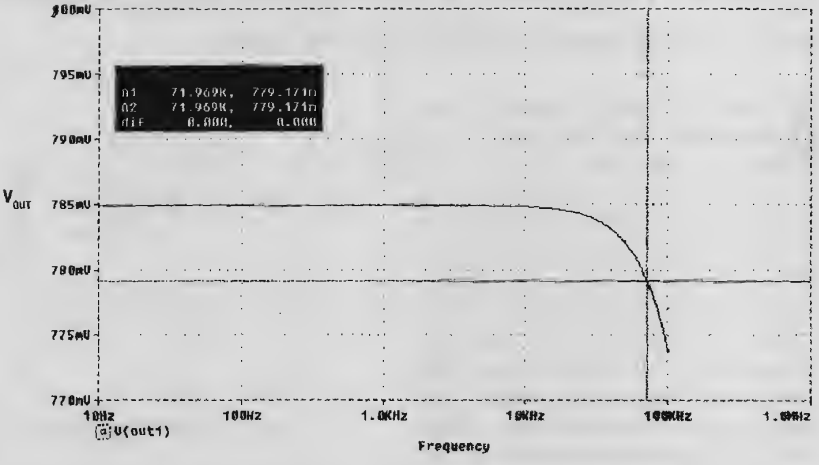
$$L_2 = \frac{L_P}{n^2};$$

Figure 1



Spice models simulate an ideal transformer (a) and a nonideal one (b).

Figure 2



A Spice simulation yields the transfer function of the nonideal transformer described in the text.

$$L_S = L_P\left(\frac{1}{k^2}2\right);$$

$$n = k\left(\sqrt{\frac{L_1}{L_2}}\right).$$

Then, if you know the L_P and L_S values, you also know the coupling factor, k. L_1 is the inductance measured at the operating frequency between terminals In_1 and In_2 with no load connected between Out_1 and Out_2. Similarly, L_2 is the inductance measured at the operating frequency between terminals Out_1 and Out_2 with no load connected between In_1 and In_2. L_S is the inductance measured at the operating frequency between terminals In_1 and In_2 with Out_1 and Out_2 short-circuited. From these values, using the previous **equations**, we obtain the parameters of the equivalent circuit in **Figure 1b. Listing 1** shows the PSpice subcircuit that represents the behavioral model of a nonideal transformer. You can use the subcircuit for both transient and ac analysis.

LISTING 1—SPICE SIMULATION OF NONIDEAL TRANSFORMER

```
.SUBCKT transformer in1 in2 out1 out2 params: L1=1u L2=1u Ls=1u

R_Rs      in1 1  1n

L_Ls      1 2 {Ls}

L_Lp      in2 2  {L1-Ls}

E_E1      3 out2 VALUE { (sqrt(L2/(L1-Ls)))*V(2, in2) }

V_Vsense  out1 3 0V

F_F1      4 0 V_Vsense 1

R_Rload    4 0  0.1n

G_G1       2 in2 VALUE { ((10G)*sqrt(L2/(L1-Ls)))*V(4, 0) }

.ENDS     transformer
```

The input parameters of the subcircuit are the measured values of inductances L_1, L_2, and L_S. You obtain the ideal transformer, T, by means of the voltage-controlled voltage source, E_1, and the voltage-controlled current source, G_1, connected back to back (**Reference 1**). The current source, G_1, senses the current, $I(V_{sense})$, and provides the current $I(V_{sense})/n$. The transformation ratio n is a function of inductances L_1, L_2, and L_S.

As an example, consider a transformer that provides an impedance transformation of 46 to 75Ω at 72 kHz. It uses an RM8 ferrite core with inductance factor A_L=1600 nH. The measured inductances are L_1=4.2 mH, L_2=2.6 mH, and L_S=20 μH. **Figure 2** shows the simulated transfer function of the transformer. You can download **Listing 1** from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2539. (DI #2539).

REFERENCE

1. Coelho, J, "A Spice model for the ideal transformer," *Electronic Design*, June 28, 1999.

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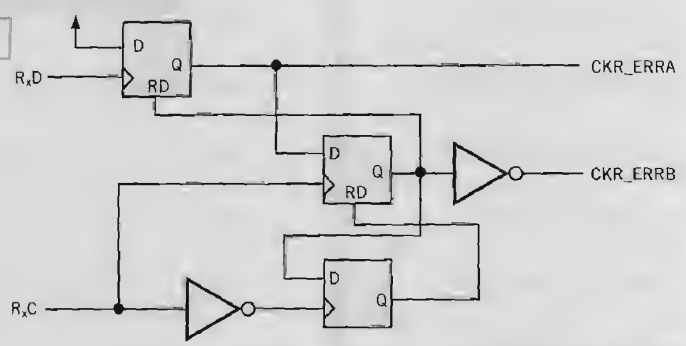
Clock-recovery scheme suits low-SNR systems

Luis Miguel Brugarolas, SIRE, Madrid, Spain

A CLOCK-RECOVERY ARCHITECTURE can operate with NRZ digital signals, even at low SNRs. A clock-recovery subsystem is based on a PLL comprising a phase comparator, a loop filter, and a voltage-controlled oscillator (VCO). If you place the phase comparator after the demodulator block, a typical criterion for comparison is the zero crossings of the received signal (the edges of a TTL-compatible signal). The phase comparator must provide a voltage proportional to the phase difference between the incoming signal and the local-

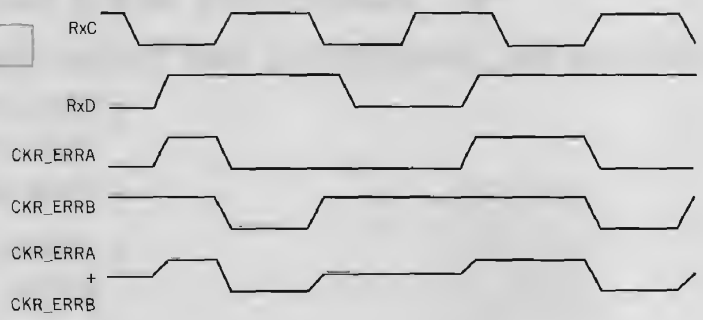
Figure 1



A programmable-logic IC forms the phase comparator for the clock-recovery system.

ly generated clock (the VCO output). But, in comparison with a synthesizer-based phase comparator, the comparison must take place only when information exists; that is, at data-level transitions. The recovery system should disable the phase comparator in the absence of data-level transitions to minimize comparator noise. **Figure 1** shows a phase comparator you can implement in a CPLD or an FPGA. Tests show that the comparator works successfully in a 2-Mbps V_{SAT} demodulator with SNR of 6 dB and lower. The comparator can easily acquire and track the signal.

Figure 2



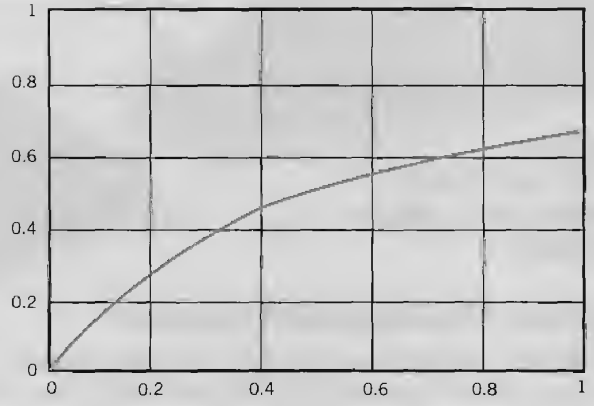
The last waveform represents the absolute value of the difference between CKR_ERRA and CKR_ERRB.

The phase comparator uses three D-type flip-flops with asynchronous reset inputs. The comparator has two inputs: RxD and RxC, and two outputs: CKR_ERRA and CKR_ERRB. These inputs and outputs form a three-level output, both high for increasing frequency, both low for decreasing frequency, and both at different levels for no change in frequency. They form a state machine:

1. Data rising edge triggers CKR_ERRA.
2. Once triggered, next RxC rising edge triggers CKR_ERRB and resets CKR_ERRA.
3. Next RxC falling edge (thus, a half-clock period later) resets CKR_ERRB.

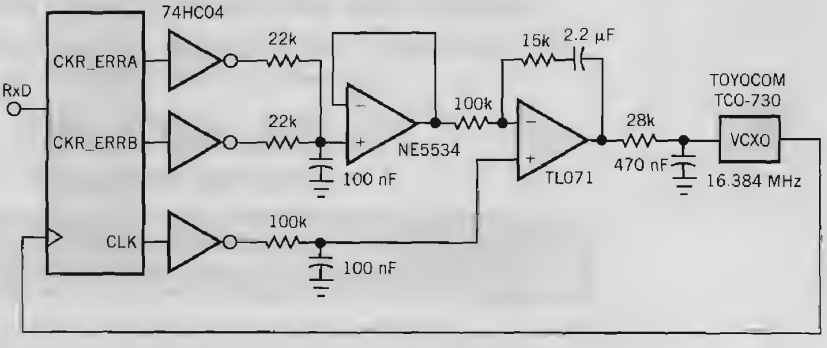
Figure 2 shows the operation of the phase comparator. The transfer function is not linear (**Figure 3**). It corresponds to the expression $V_{OUT} = t/(1+T/2)$, where t is the time from RxD's rising edge to RxC's rising edge, and T is the period of RxC. The nonlinear transfer function is not a limitation, because the system operates around the point at which t=T/2. Moreover, the presence of noise effectively reduces the comparator's gain and smoothes its operation. Thus, the PLL's design must accommodate variations in the comparator's transfer function. **Figure 4** shows a simplified final PLL implementation. The programmable-logic device uses buffering to attenuate the digital switching noise of the device. The op amp's noninverting reference input comes from the filtered symmetrical clock signal; thus, the reference level is exactly centered between the low and high logic-level voltages. The system is thus voltage-independent. (DI #2740)

Figure 3



The phase comparator's output is nonlinear; however, the nonlinearity is inconsequential to the clock-recovery function.

Figure 4



The complete clock-recovery circuit uses a small handful of components.

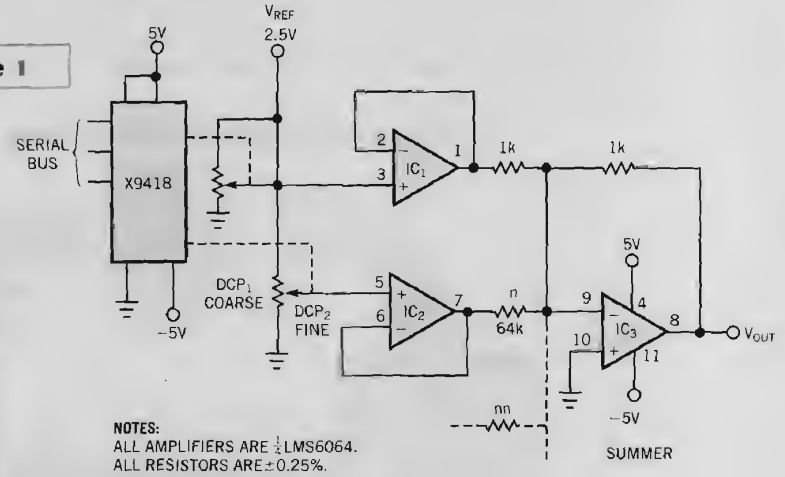
For This Design, Circle No. 501

Op amp increases potentiometer's resolution

Chuck Wojslaw, Xicor Inc, Milpitas, CA, and P Gareth Lloyd, Elab Ltd, Stoke-on-Trent, UK

A KEY PARAMETER of digitally controlled potentiometers (DCPs) is the number of taps (n) programmable positions of the wiper. This parameter establishes the resolution in programmable-voltage and -current applications. A number of circuit techniques exist for improving the resolution using one or more DCPs with a given number of taps. The circuit in **Figure 1** has no theoretical limit on increasing the resolution in programmable-voltage applications. The IC_3 amplifier circuit is an inverting summer with weighted input-resistor values. The input voltages to the summer are the programmable output voltages of the DCPs. To reduce the effects of loading, IC_1 and IC_2 buffer the signals from the potentiometer wipers. For an n-tap potentiometer, the input resistors of the summing amplifier are R and nR, providing a programmable output voltage of $0V > V_{OUT} > -V_{REF}(1+1/n)$, with a resolution of $V_{OUT}(smallest) = -V_{REF}/[n(n-1)]$.

Figure 1



The sky's the limit on resolution in this programmable-voltage circuit.

For the dual 64-tap Xicor X9418 DCP and the circuit values shown, the output voltage, V_{OUT}, has n^2, or 4096, programmable values. The full-scale value is 2.5391V, and the smallest programmed voltage is 0.62 mV. You can program the coarse DCP_1 from 0 to 2.5V with a resolution of 39 mV, and you can program the fine DCP_2 from 0 to 39 mV with a resolution of 0.62 mV. This circuit provides the same resolution as a 12-bit D/A converter. Measured data fell within 2 LSBs of calculated values. Adding more potentiometers, buffers, and input resistors provides theoretically unlimited resolution. If you add a third section, the resolution increases to one part in 262,144 (18 bits). You can implement a similar scheme using a noninverting summer circuit. You can use the circuit as a substitute for expensive D/A converters in any application that requires a precise, high-resolution programmable voltage. (DI #2537).

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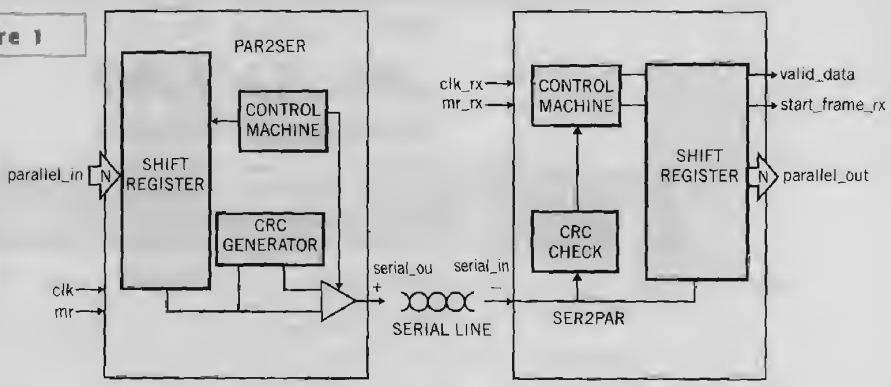
VHDL customizes serializer/deserializer

Antonio Di Rocco, Siemens ICN, L'Aquila, Italy

MANY APPLICATIONS require a multiple-signal exchange among cards through a backplane. Several solutions are available to serialize/deserialize data—from the classic UART to newer low-voltage differential-signaling components. It is sometimes important to have hardware flexibility in

Figure 1



Using VHDL, you can customize a PLD to perform serialization and deserialization.

transferring signals; for example, you can use a PLD to implement a UART-like function to perform a parallel-serial-parallel conversion (**Figure 1**). **Figure 2** shows the frame structure. The idle "1" bits exactly fill the time between the start and stop bits. Assuming $f_{BIT}=1/T_{BIT}$ as the speed of the serial link, the sampling frequency, f_{SH}, for each parallel-input channel is $f_{SH}=f_{BIT}[(N+3)/2]$. With an internal state machine working with a system clock (clk), each eight-clock period corresponds to one bit period, T_{BIT}. The relationship between sampling frequency f_{SH} and the PLD clock is $f_{SH}=[f_{CLK}(N+3)]/4$.

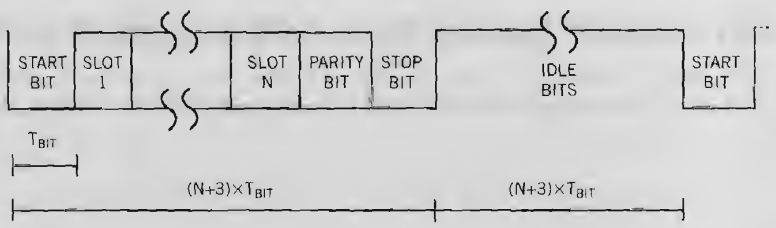


Figure 2 The system in Figure 1 produces this frame structure.

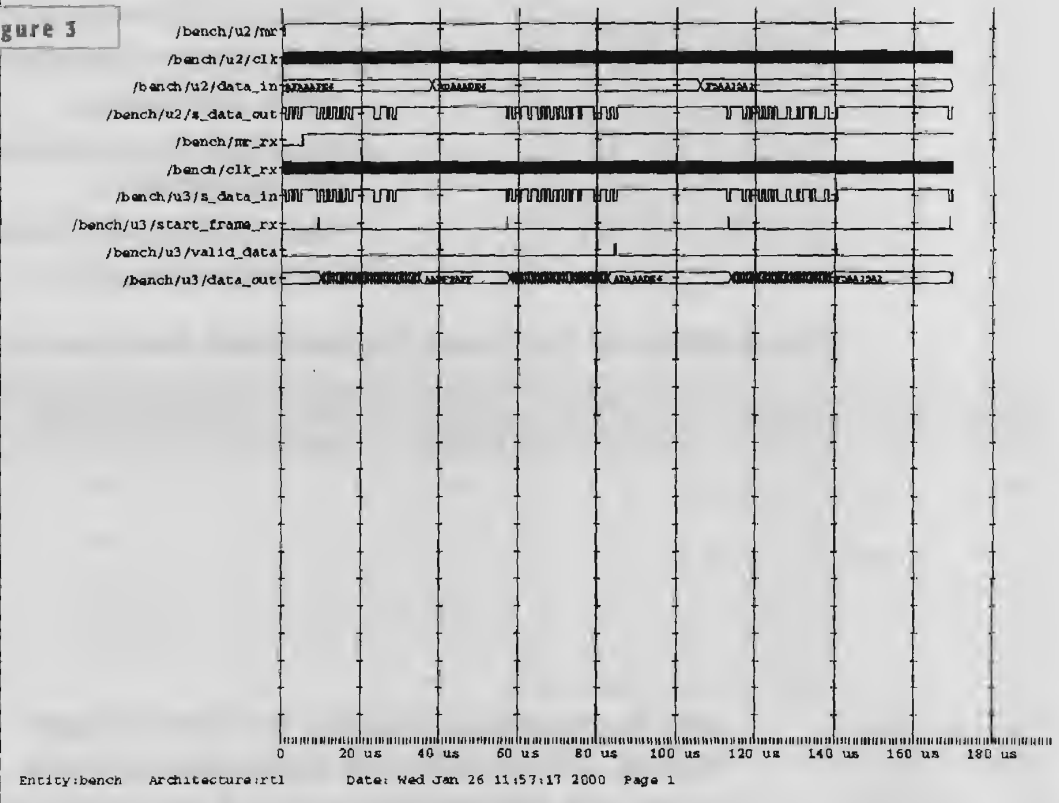


Figure 3 Simulation yields this serialization pattern for 32 parallel-input channels.

The deserializer does not perform a clock-recovery function but works with the nominal clock frequency of the transmitter side. Jitter tolerance on the serial line is related to the number of parallel-input channels. During the time between the start bit and the stop bit, the system tolerates a delay time of $^3/_8T_{BIT}$. Often, system features are related to the maximum speed the serial link allows. To improve the quality of transmission, you can insert a more complex CRC function. The timing simulation shows a serialization of N=32 signals using a sampling frequency $f_{SH}=17.8$ kHz, which corresponds to a PLD clock $f_{CLK}=10$ MHz with a speed of 1.25 Mbps on the serial link (**Figure 3**). Note that the serializer's start bit occurs just as the master reset (mr_rx) is deasserted. On the receiver side, the deserializer has its master reset (mr_rx) deasserted while it receives a frame; thus, it starts to sample a wrong frame. Between the two first start_frame_rx pulses, no valid_data pulse exists. The frame-acceptance pulse appears at the end of the second received frame. You can easily customize the VHDL code. It uses the ser2par.vhd and par2ser.vhd component source files. Another VHDL listing has the package source file, in which the constant N designates the number of parallel channels. Finally, a "bench" routine, bench.vhd, runs simulations. You can download the VHDL listings from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2542. (DI #2542).

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Sometimes, one capacitor is better than two

Robert LeBoeuf, National Semiconductor, Salem, NH

Many A/D converters use an internal resistor ladder as a two-point differential voltage reference in the conversion. This method demands that these two nodes remain steady. The higher the resolution, the stronger the demand for quiet voltages. **Figure 1** depicts a simplified schematic of the LM985XX reference ladder. **Figure 1a** shows the traditional decoupling scheme; **Figure 1b** shows a proposed scheme. Typically, designers use two capacitors to decouple each reference node—one low-value capacitor and one of higher value because the effective series inductance (ESL) of the smaller capacitor is much lower than that of the larger one. Contrary to tradition, you can eliminate these larger capacitors and replace them with one differential capacitor if you choose the values wisely. Because the difference in the reference voltages, ΔV_{REF}, is important in conversion, this is the delta that is of interest.

Figure 1b shows two common-mode decoupling capacitors, C_1 and C_2, and the differential capacitor, C_3. The current sources, I_1 and I_2, represent the average currents pushing or pulling on the ladder. These currents are generally proportional to the input voltage, V_{IN}, and the sampling frequency, f. If the input voltage is periodic or at least quasiperiodic, then you can choose the decoupling capacitors on the basis of the maximum ripple voltage allowed to appear differentially on the nodes. This ripple specification is based on the permissible output error. The poles and zero of the transfer function are, respectively,

$$pole_1 = \frac{-1}{2} \cdot \frac{(C_2 \cdot R_{P3} \cdot R_{P1} + C_3 \cdot R_{P2} \cdot R_{P1} + C_1 \cdot R_{P2} \cdot R_{P3})}{[(C_2 \cdot C_3 + C_1 \cdot C_3 + C_1 \cdot C_2) \cdot R_{P2} \cdot R_{P3} \cdot R_{P1}]} \cdot \delta;$$

$$pole_2 = \frac{1}{2} \cdot \frac{(C_2 \cdot R_{P3} \cdot R_{P1} + C_3 \cdot R_{P2} \cdot R_{P1} + C_1 \cdot R_{P2} \cdot R_{P3})}{[(C_2 \cdot C_3 + C_1 \cdot C_3 + C_1 \cdot C_2) \cdot R_{P2} \cdot R_{P3} \cdot R_{P1}]} \cdot (\delta - 2);$$

$$(\delta << 1)$$

$$ZERO = \frac{R_2 + R_1}{R_2 \cdot R_1 (C_1 + C_2)}, \text{ and } R_{PK} = \frac{R_n \cdot R_m}{R_n + R_m},$$

where k, n, and m are cyclic permutations of 1, 2, and 3. You can easily see that the pole in the first **equation** is the dominant pole. As long as the zero is sufficiently far from $pole_1$, then this pole (hence, C_3) determines the roll-off. If C_1 and C_2 are small enough, the zero finds itself well away from $pole_1$. Using the values in **Figure 1b**, the poles and zero become $pole_1 = -28.50$ Hz; $pole_2 = -3.948 \times 104$ Hz; and zero $= 2.48 \times 105$ Hz.

Typically, the current sources have a fundamental frequency equal to the frequency of the analog clamp. The most pessimistic assumption is that the input signal contains all white pixels. This scenario causes the maximum swing in the current sources and the smallest duty cycle. Using this assumption and a current amplitude of 0.6 mA, the capacitor values shown in **Figure 1b** would produce $\Delta V_{REF} = 1.989$ mV. Instead, if you used a pair of 12-µF decoupling capacitors, as in **Figure 1a**, the circuit would produce $\Delta V_{REF} = 3.975$ mV. (DI #2543)

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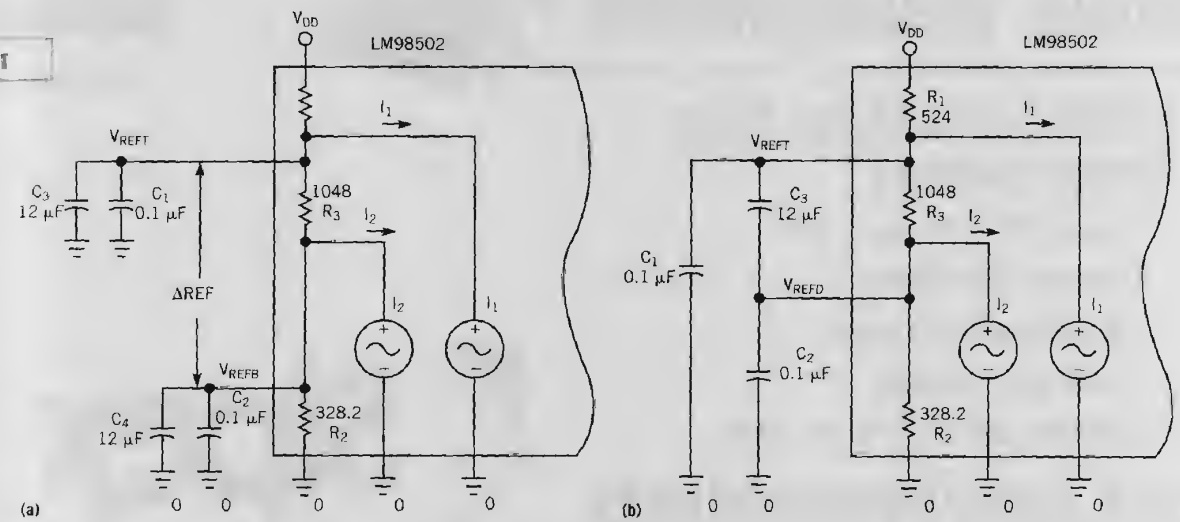
Figure 1



More is not always better; the circuit in b provides better decoupling than the one in a.

Inverter offers design flexibility

Nihal Kukaratna, Arthur C Clarke Institute, Katubedda Moratuwa, Sri Lanka

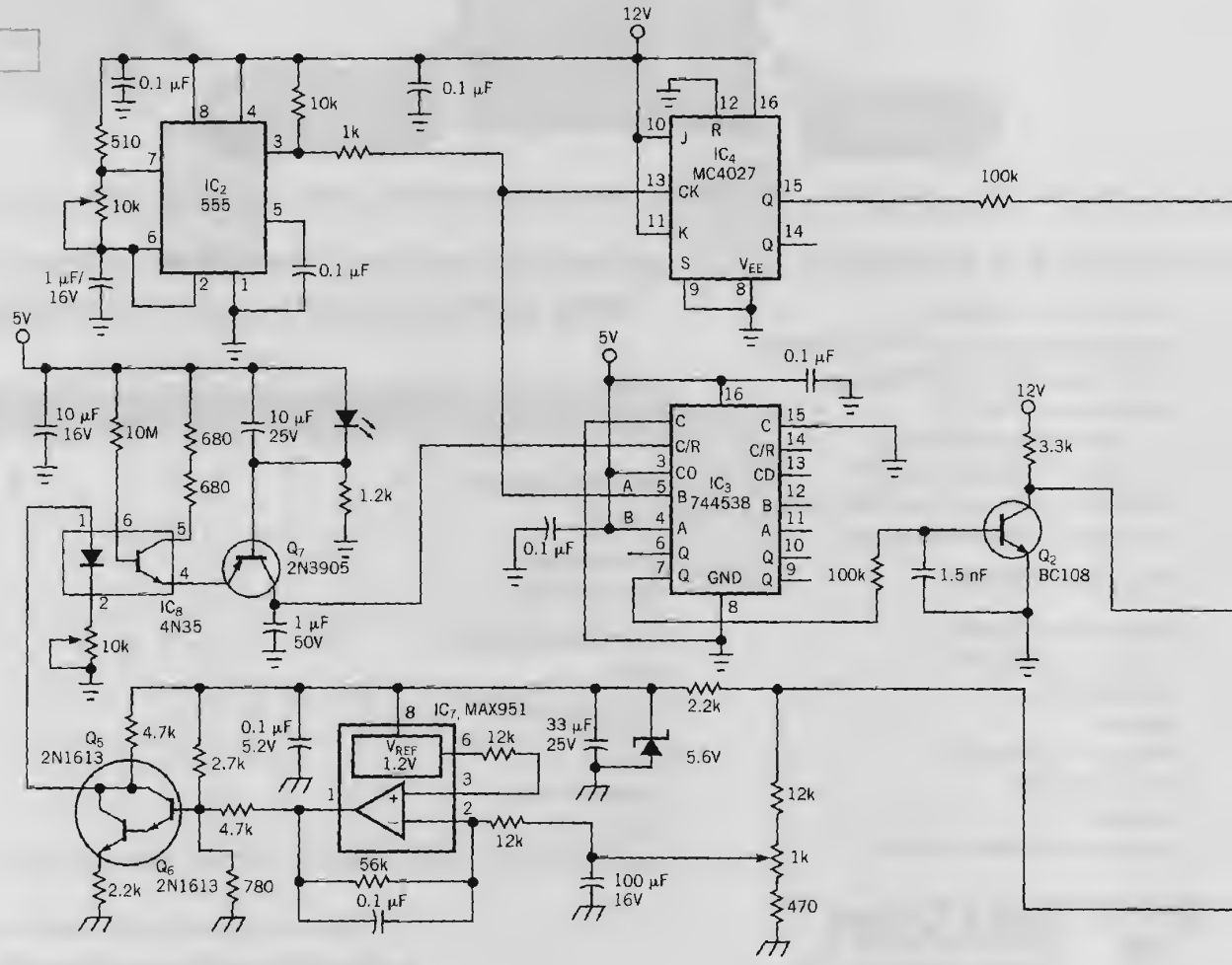
You may occasionally need a substitute for a commercial dc/ac inverter. A typical application is in an uninterruptible power supply (UPS). The circuit in **Figure 1** is a flexible, low-component-count inverter with closed-loop voltage regulation. The advantages of the circuit are that it works from a 12V car battery (or from higher battery voltages with minor modifications), it offers closed-loop voltage regulation, and phase locking with a commercial power supply is possible.

The circuit is designed around a MOS-gate driver family, such as International Rectifier's (www.irf.com) IR215X family (IC_5). This IC drives the gates of power MOSFETs Q_3 and Q_4 through NAND gates (IC_6). A 555-timer-based 100-Hz oscillator (IC_2) feeds the MOS-gate driver's frequency-generation block through a divide-by-two circuit (IC_4). The MOS-gate drivers' low and high outputs drive the power MOSFETs' gates through IC_6. The combination of the MOS-gate driver and the IC_6 NAND gates maintains the necessary deadband to prevent simultaneous conduction of the power-MOSFET pair. A voltage-feedback sample, compared with the 1.2V reference source in a MAX951, IC_7, provides a closed-loop feedback to vary the value of the constant-current source comprising Q_7 and the optoisolator, IC_8. This variable constant-current source varies the monostable output of IC_3, which feeds the IC_6 NAND gates. The feedback system thus maintains the proper pulse width in the gate drivers.

You can easily modify the (square-wave) circuit for a sinusoidal output by

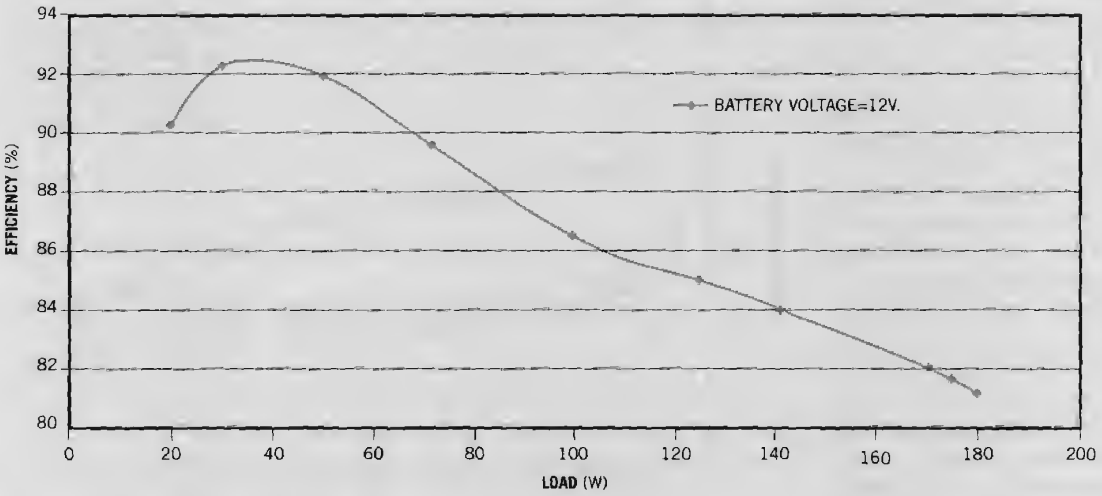
(text continued on pg 174)

Figure 1

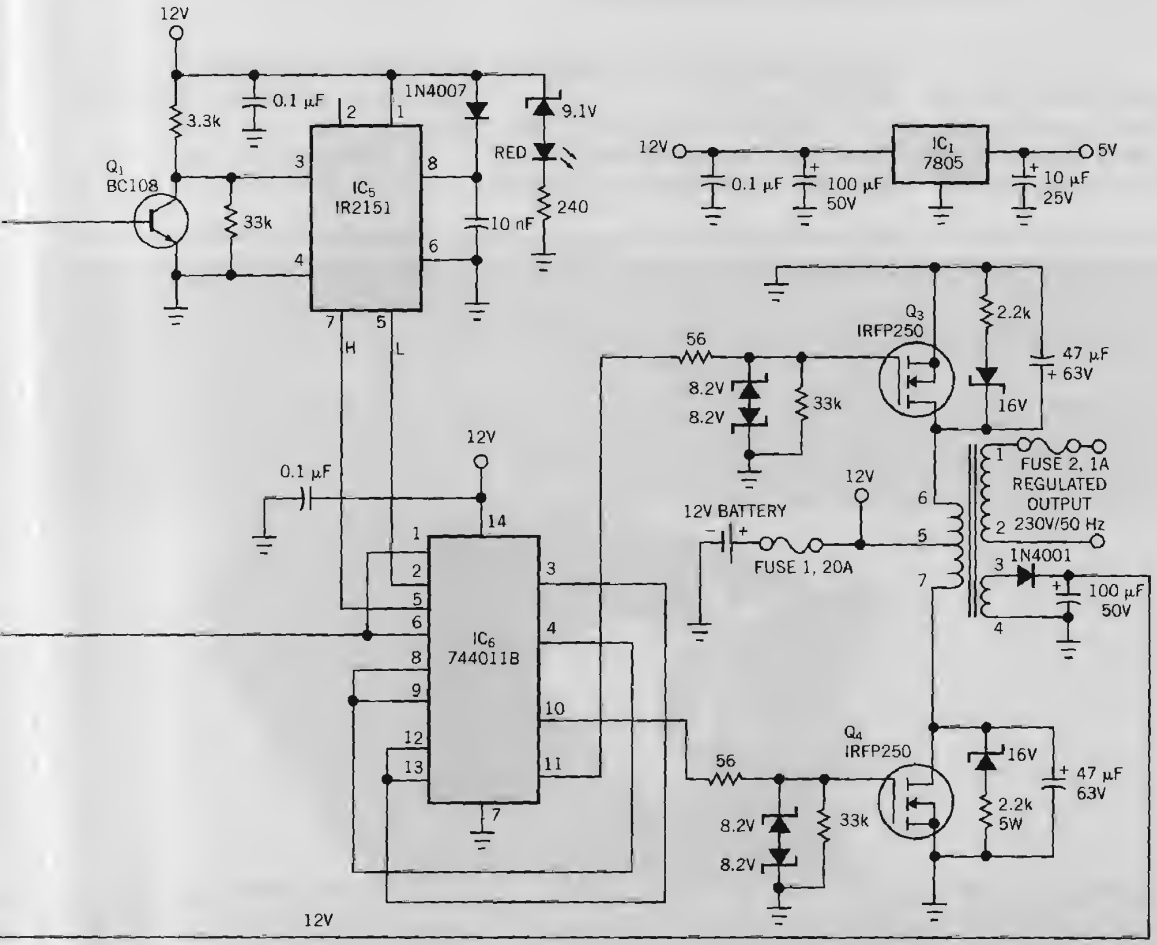


Roll your own dc/ac inverter, using a MOS-gate driver IC.

Figure 2

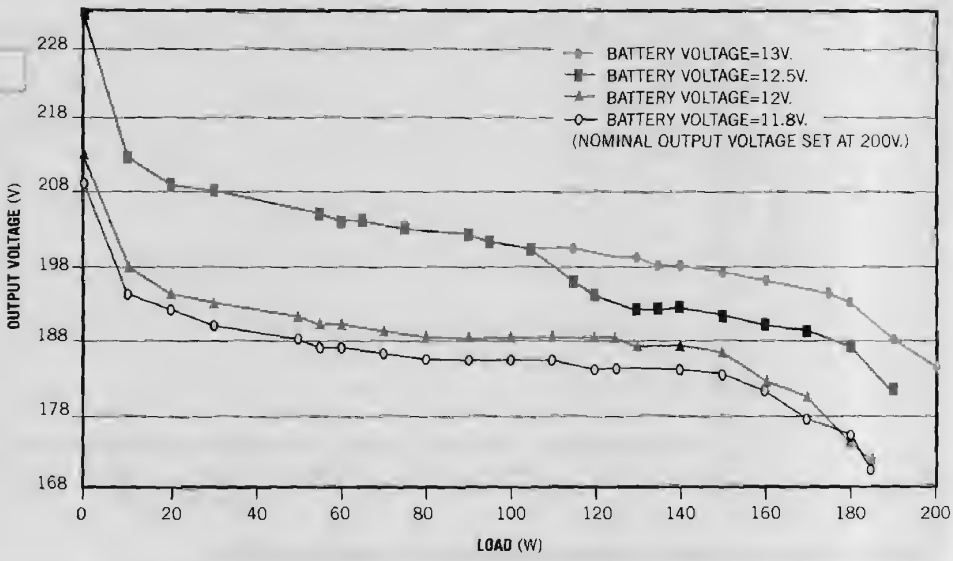


The circuit in Figure 1 maintains reasonably tight regulation for a wide range of loads.



adding a few components between IC_3 and IC_6 (**Reference 1**). For higher outputs, you need change only the battery voltage and the power MOSFETs. The circuit in **Figure 1** is a 200-VA unit. **Figure 2** shows the output-regulation curve for different battery-voltage inputs. **Figure 3** shows the efficiency-versus-load curve. The inverter circuit has 81 to 93% efficiency for loads of 15 to 180W. Using a tape-wound, powdered-iron-core transformer as T_1, you can package the unit in a 100-in.^{3} volume for a 230V, 50-Hz emergency power source. (DI #2538).

Figure 3



Efficiency peaks at nearly 93% for moderate loads.

REFERENCES

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2. N Kularatna and M de Silva, "DSP-Based Sine-Wave Inverters for UPS and Emergency Power Supplies with MOS Gate Drivers," Proceedings of Power Systems World Conference (PCIM 99), pg 296.

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